## AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0011], Page 4 at line 5 of the specification as follows:

[0011] wherein the first differential amplifier circuit receives an input signal via the first resistor and inputs an output signal to the second and third differential amplifier circuit via the second resistor, the second differential amplifier circuit drives one of the first and the second transistor, the third differential ~~transistor~~ amplifier circuit drives the other of the first and the second transistor, and an output signal of the output stage circuit is fed back to an input of the first differential amplifier circuit via the first feed back resistor and to inputs of the second and the third differential amplifier circuit via the second feed back resistor.

Please amend paragraph [0013], Page 4 at line 24 of the specification as follows:

[0013] Further, the respective differential amplifier circuits are operated at a source voltage with respect to a reference potential (ground) or at a voltage between the voltages. Thereby, a drive signal for the output stage circuit can be produced with a comparatively low voltage. Further, a double feed back circuit in which the output signal of the output stage circuit is fed back to the first ~~differential circuit~~ differential amplifier circuit as well as to the inputs of the second and the third differential amplifier circuit is constituted.

Please amend paragraph [0032], Page 10 at line 19 of the specification as follows:

[0032] In the present embodiment, the transistor Trp is driven by a voltage signal less than +VDD/2 among input signals of the differential amplifier circuit 2 and is

turned off, when the voltage signal exceeds +VDD/2. On the other hand, the transistor Trn is driven by a voltage signal exceeding +VDD/2 among input signals of the differential amplifier circuit 3 and is turned off, when the voltage signal ~~exceeds~~ becomes less than +VDD/2. Thereby, the output terminal 5a of the audio output circuit 10 generates a push-pull output.

Please amend paragraph [0038], Page 12, at line 30 of the specification as follows:

[0038] The bias line Vs is a line of a constant voltage taken out from a connection point between a constant voltage circuit 8 and a current source 7. Between the power source line +VDD and the ground GND the current source 7 and the constant voltage circuit 8, which receives a current from the current source 7 at the downstream thereof are disposed being connected in series. The constant ~~current~~ voltage circuit 8 is constituted by a series circuit of a diode connected transistor and a resistor.